IN THE CLAIMS

The following is a complete listing of the pending claims:

1. (previously presented) An application specific integrated circuit (ASIC) conversion of a programmable logic device (PLD), wherein the programmable logic device comprises a plurality of PLD logic blocks and a PLD routing structure operable to couple logical inputs to each PLD logic block, comprising:

a plurality of ASIC logic blocks corresponding on a one-to-one basis with the plurality of PLD logic blocks; and

an ASIC routing structure configured to couple logical inputs to each ASIC logic block, wherein the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure, and wherein the ASIC routing structure is adapted to be delay matched to propagation delays in the PLD routing structure.

2. (original) The ASIC conversion of claim 1, wherein the PLD logic blocks and the ASIC logic blocks are lookup table (LUT)-based logic blocks.

3. (original) The ASIC conversion of claim 1, wherein the PLD logic blocks and the ASIC logic blocks are programmable AND array-based logic blocks.

4. (original) The ASIC conversion of claim 2, wherein the ASIC includes a plurality of metal layers; wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias each selected so as to provide either a logic high or a logic low value to the plurality of ASIC logic blocks to provide the same truth tables as used in the PLD logic blocks.

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5. (original) The ASIC conversion of claim 2, wherein the ASIC includes at least one metal layer, wherein traces formed in the metal layer are customized to provide the same truth tables for the ASIC logic blocks as are used in the PLD logic blocks.

6. (original) The ASIC conversion of claim 4, wherein only the first and second metal layers are coupled by vias selected so as to provide either a logic high or a logic low value to the plurality of ASIC logic blocks to thereby provide the same truth tables as in the PLD logic blocks.

7. (original) The ASIC conversion of claim 4, wherein the first metal layer includes traces carrying voltage levels VCC and VSS, and wherein the vias are selected to couple to VCC to provide a logic high value and to couple to VSS to provide a logic low value.

8. (original) The ASIC conversion of claim 1, wherein the ASIC includes a plurality of metal layers, and wherein at least a first metal layer and a second metal layer in the plurality are coupled by vias each selected so that the coupling provided by the ASIC routing structure routing structure is the same as that provided by the PLD routing structure.

9. (original) The ASIC conversion of claim 8, wherein the PLD routing structure is a buffered, segmented routing structure, each buffered PLD routing segment corresponding to an ASIC buffered routing segment, and wherein the vias are each selected so that the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure on a segment-by-segment basis.

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10. (previously presented) The ASIC conversion of claim 9, wherein the adaptation of the ASIC routing structure to be delay matched comprises, for each ASIC routing segment, a diode load coupled through a via provided between the first and second metal layer to match the propagation delay in the corresponding PLD routing segment.

11. (previously presented) The ASIC conversion of claim 9, wherein the buffers in each PLD routing segment are constructed with transistors having one of a plurality of channel widths, the selected channel width affecting the propagation delay through the buffer, and wherein the adaptation of the ASIC routing structure to be delay matched comprises a plurality of programmable buffers, each programmable buffer operable to match the propagation delay in a corresponding buffer in the PLD routing structure.

12. (original) The ASIC conversion of claim 11, wherein each programmable buffer comprises a plurality of inverters operable to be selectively coupled in parallel.

13. (original) The ASIC conversion of claim 12, wherein the plurality of inverters comprises three inverters.

Claims 14 through 16. (cancelled)

17. (previously presented) An application specific integrated circuit (ASIC) conversion of a programmable logic device (PLD), wherein the programmable logic device comprises a plurality of PLD logic blocks configured to perform a desired task and a PLD routing structure operable to couple logical inputs to each PLD logic block, comprising:

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a plurality of ASIC logic blocks corresponding on a one-to-one basis with the plurality of PLD logic blocks;

an ASIC routing structure configured to couple logical inputs to each ASIC logic block, wherein the coupling provided by the ASIC routing structure is the same as that provided by the PLD routing structure, and wherein the ASIC routing structure is adapted to be delay matched to propagation delays in the PLD routing structure; and

means for configuring the plurality of ASIC logic blocks to perform the desired task.

18. (original) The ASIC conversion of claim 17, wherein the ASIC includes a plurality of metal layers, and wherein the means for configuring the plurality of ASIC logic blocks includes a plurality of vias between at least a first metal layer and a second metal layer, each via being positioned so as to provide either a logic high or a logic low value to an ASIC logic block, the plurality of vias thereby supplying the same truth tables as used in the PLD logic blocks.

19. (original) The ASIC conversion of claim 17, wherein the means for configuring the plurality of ASIC logic blocks includes a plurality of conductors within at least one metal layer of the ASIC, each conductor being positioned so as to provide either a logic high or a logic low value to an ASIC logic block, the plurality of conductors thereby supplying the same truth tables as used in the PLD logic blocks.

20. (original) The ASIC conversion of claim 18, wherein the routing structure in the programmable logic device is a buffered, segmented routing structure, each buffered PLD routing segment corresponding to an ASIC buffered routing segment.

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Claims 21 through 31 (cancelled).

32. (original) An application specific integrated circuit (ASIC) comprising:

a plurality of logic blocks corresponding to programmable logic blocks of a programmable logic device (PLD); and

a routing structure corresponding to the programmable routing structure of the PLD but having permanently formed connections therein, the ASIC routing structure adapted to produce a signal propagation delay that matches substantially the signal propagation delay in the corresponding PLD programmable routing structure.

33. (original) The ASIC of claim 32, wherein the permanently formed connections of the ASIC routing structure include selectively formed vias between conductive layers to provide a desired route through the routing structure.

34. (original) The ASIC of claim 32, wherein the permanently formed connections of the ASIC routing structure include selectively formed vias between conductive layers to produce a desired capacitive load on the routing structure

35. (original) The ASIC of claim 34, wherein the desired capacitive load is provided by a programmable diode formed in a conductive layer.

36. (original) The ASIC of claim 32, wherein the permanently formed connections of the ASIC routing structure include a buffer permanently programmable to provide a desired signal propagation delay through the buffer.

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37. (original) The ASIC of claim 36, wherein the programmable buffer comprises a plurality of programmable inverters arranged in parallel.

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